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(54) CMOS Syncronous rectifier circuit for step-up devices.

(57) A DC/DC converting circuit adapted to convert a DC input voltage (Vin) to a DC output voltage (Vout) uses, as its synchronous rectifier member, a bipolar power transistor (21) of the PMOS type, and allows it to be turned on by a control logic circuit (24) capable of quickly sensing automatically the difference in electric potential between a conduction terminal and the body terminal of the transistor.

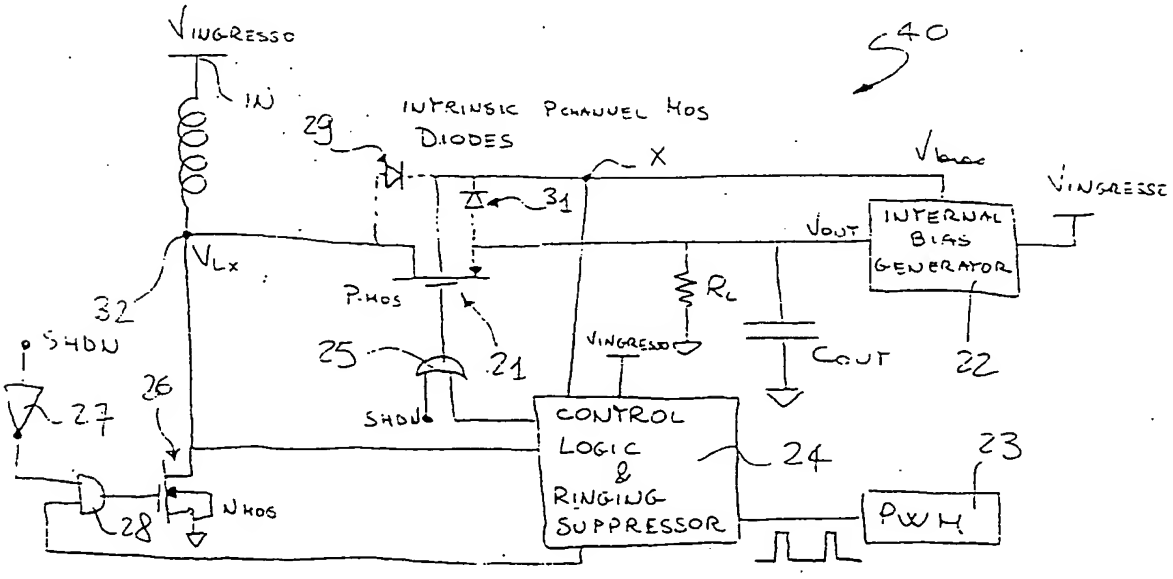

Fig. - 4

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Description

Field of the Invention

[0001] This invention relates to a synchronous CMOS rectifying circuit for step-up devices.

[0002] The invention also relates to a method of carrying out a DC/DC conversion by means of the above circuit.

[0003] More particularly, the invention deals with a family of high-efficiency synchronous circuits for switching control which can be operated in the step-up mode even at very low (around 0.8V) supply voltages and very small idle currents.

[0004] Considerable research work is being conducted in this specific field to develop synchronous rectifying circuits, specifically for step-up devices, which can be operated at very low (e.g. 0.8V) supply voltages and very small idle currents.

[0005] The demand for rectifiers with such features comes especially from those applications where battery-powered apparatus, such as pagers, cellular phones, portable computers, and more generally long-range portable apparatus, require that the conversion of a battery voltage to a stabilized voltage of a higher value be carried out in a most efficient manner.

[0006] A general trend in the design of such rectifiers provides for the use of active switch elements having very low internal resistance and a high switching rate. and the use. as active elements, of field-effect transistors or bipolar transistors in place of the loop-back diodes employed in the past. The class of converters thus produced are known as synchronous rectifying converters. also on account of a control logic being provided therein which is effective to perfectly sychronize the opening and closing of the switch elements and prevent simultaneous activation (cross-conduction) from occurring as would result in large power dissipation or unacceptably poor performance.

[0007] A synchronous rectifying circuit ideally should be capable of operating with very low supply voltages and of minimizing cross-conduction losses as the switch elements are turned on simultaneously.

[0008] Additional features expected of such an ideal rectifier include those summarized herein below:

should produce full disconnection of the output load from the electrical source in a shut-down situation and with an output voltage Vout=0:

should dampen out the oscillation that appears as the inductor is fully discharged due to the presence of parasitic capacitances in the switch elements (damped ringing):

should enhance the converting efficiency of the circuit:

should automatically clamp the internal supply voltage of the circuit to the highest available potential (self-bootstrapping).

Prior Art

[0009] Shown by way of example in Figure 1 is a schematic diagram of a prior art synchronous rectifying circuit 20 as applied to a step-up topology. The circuit has an input terminal IN which is supplied a voltage Vin, and has an output terminal OUT which is connected to an electric load. The circuit 20 uses a P-channel Power-MOS 11 for a switch element. A control logic 13 controls the sequencing and times the actuations of the switches 14 and 11 through respective outputs 16 and 17. By using an active switch element 11, a smaller voltage drop can be obtained in transferring power to the load.

[0010] A sensing element 18 adapted to sense the current being transferred to the load is provided for a compare block 12, which is arranged to control the transfer of power and send a suitable signal to the control logic 13 through an input 15.

[0011] The signal from the compare block 12 effectively prevents the Power-MOS 11 from also transferring power from the load to the input IN, thus reversing the current direction and defeating all attempts at improved efficiency.

[0012] The determination to use a P-channel Power-MOS for a switch element is justified by the low internal resistance of Power-MOSs and the ability to use a voltage-oriented rather than current-oriented drive. Unfortunately. the presence of the Power-PMOS body connection introduces. as shown in Figure 1. a large-size diode across the input and output terminals of the circuit 20. At start-up, when the output voltage is still close to zero, this large diode allows an inrush of current whose maximum value can be far above the peak value during steady-state operation and which has detrimental effects on the passive components (inductor 18). unless the latter are provided oversize to accommodate this initial transient phase.

[0013] An attempt to depress the maximum value of the inrush current by the use of a limiting resistor admittedly would safeguard the components. but also result in unacceptably large power losses.

[0014] Lastly. the presence of the parasitic diode makes adjusting the output voltage to values below Vin-V_{BE} (step-down configuration) impracticable.

[0015] Another approach to providing a highly efficient synchronous rectifier is shown in Figure 2 and described in European Patent Application No. 97830740.3 by this Applicant.

[0016] Shown in that Figure is a synchronous rectifier 30 which comprises a bipolar transistor 7 as a switch element. A rectifier block 2 includes a control logic 5 which is connected to all the terminals 3. 4 of the transistor 7 and receives the supply voltage Vin on an input 6.

[0017] A second switch element 1 is provided which is formed with MOS technology and incorporates a control logic 10.

[0018] While in many ways advantageous, this solution is inadequate to remove all the ringing and minimize the losses from cross-conduction.

[0019] A further prior approach is shown schematically in Figure 3. This is a synchronous rectifying circuit 19 manufactured by Maxim Semiconductors. This circuit cannot be operated at lower voltages than 1.7V.

[0020] To summarize, all of the prior art solutions, although providing highly efficient step-up converters, still have limitations and deficiencies, including complex control logic circuitry, inability to operate with low supply voltages, possible cross-conduction side effects, and inability to operate in a step-up/step-down combined mode.

[0021] The underlying technical problem of this invention is to provide a high-efficiency rectifying circuit, particularly indended for step-up/step-down applications, which is of uniquely simple construction and affords outstanding performance in terms of ringing suppression and full disconnection of the load in the shut-down mode.

Summary of the Invention

[0022] The concept behind this invention is one of using, as the gist of the synchronous rectifier, a MOS type of power transistor which can suppress the ringing effect and ensure full shutting down of the load.

[0023] Based on this concept, the technical problem is solved by a synchronous rectifying circuit, specially useful with step-up devices, as previously indicated and defined in Claim 1 appended hereto.

[0024] The invention also relates to a method as previously indicated and defined in Claim 10.

[0025] The features and advantages of a circuit and method according to this invention will become apparent from the following detailed description of an embodiment thereof, given by way of example and not of limitation with reference to the accompanying drawings.

Brief Description of the Drawings

[0026]

Figure 1 is a schematic diagram of a DC/DC converter circuit in a step-up configuration, according to the prior art;

Figure 2 is a schematic diagram of a bipolar technology, synchronous rectifying circuit intended for a step-up type of converter, according to the prior art;

Figure 3 is a schematic diagram of yet another prior rectifying circuit;

Figure 4 is a schematic diagram of a CMOS rectifying circuit according to this invention;

Figure 5 is a circuit diagram of one embodiment of a portion of the rectifying circuit in Figure 4;

Figure 6 is a wiring diagram of a detail of the portion shown in Figure 5;

Figures 7A to 7D are plots, on the same time base, of waveforms of voltage signals which appear in the rectifying circuit of this invention in the step-up mode of operation;

Figures 8A to 8E are plots, on the same time base, of waveforms of voltage signals which appear in the rectifying circuit of this invention in a continual mode of operation;

Figures 9A to 9E are plots, on the same time base, of waveforms of voltage signals which appear in the rectifying circuit of this invention in a discontinual mode of operation;

Figures 10A to 10C are plots, on the same time base, of waveforms of voltage signals which appear in the rectifying circuit of this invention in a continual mode of operation.

Detailed Description

[0027] Referring to the drawing views, specifically to the example shown in Figure 4, a circuit diagram of a synchronous CMOS rectifier according to this invention is shown generally at 40 in schematic form.

[0028] The rectifying circuit 40 has an input terminal IN which is applied an input voltage Vin, and has an output terminal OUT whereat a rectified and stabilized DC output voltage Vout is made available.

[0029] The circuit 40 comprises the following elements:

an inductor L adapted to transfer power from the input terminal IN to the output terminal OUT;

a capacitor Cout connected between the output terminal OUT and a ground reference GND to store up energy as transferred from the inductor L;

a first electronic switch 26 adapted for coupling the inductor to the DC input voltage Vin; and

a second electronic switch 21 adapted for coupling the inductor L to the output terminal OUT.

[0030] The first electronic switch 26 is an N-channel MOS power transistor, and is controlled by a control circuit 24 that handles its timing through a logic gate 25

receiving a signal SHDN on one input via an inverter 27.

[0031] The second electronic switch 21 has a first conduction terminal coupled to the inductor L at a node 32, and has a second terminal coupled to the output terminal OUT of the converter 40. Advantageously in this invention, the second switch 21 comprises a power transistor, preferably of the PMOS type, which has a main conduction path linking the inductor L to the output terminal. The PMOS switch 21 includes parasitic diodes 29, 31.

[0032] The control circuit 24 also drives the transistor 21 and senses the difference in electric potential between at least one of its conduction terminals, represented by the node 32, and its body terminal, represented by a bias node X. The control circuit 24 causes the power transistor 21 to conduct by activating the control terminal through a logic gate 25, which also receives the signal SHDN, when the electric potential Vlx at the node 32 is lower than the potential Vx at the body terminal X.

[0033] The control circuit 24 has an additional input terminal coupled to the input terminal IN of the converter to sense the electric potential of the input voltage Vin. This additional input terminal allows the control circuit 24 to compare the input voltage Vin with the output voltage Vout and, accordingly, operate correctly in either the step-up or the step-down mode.

[0034] In essence, the solution provided by this invention will produce a circuit 40 which can control a synchronous CMOS rectifier architecture, starting from a supply voltage which may be as low as 0.8V, and thus effect a highly efficient step-up conversion, suppress high-frequency ringing at the inductor, and ensure EMI noise reduction and power off.

[0035] The circuit 40 only employs N-channel and P-channel CMOS devices of the enhancement type using CMOS/BiCMOS technology. This circuit is specially suitable for incorporation to a step-up DC-to-DC converter.

[0036] The control circuit 24 functions to sychnronize the turning on/off of the power switches 26, 21 and to provide a shut-down condition for the circuit 40 with full disconnection of the output load.

[0037] Further provided within the logic circuit 24 is a ringing suppression circuit portion. In addition, the biasing circuit 22 functions to clamp the internal supply voltage of the whole circuit to the highest electric potential available.

[0038] Specifically, the circuit 22 receives the input voltage Vin and the output voltage Vout, and is operative to clamp -- at a node X and with minimal resistance -- the internal voltage Vbias to the highest voltage available in the circuit 40. This arrangement allows the parasitic body-drain 29 and body-source 31 diodes of the P-channel transistor 21 to be reverse biased at all times, i.e. under any conditions of operation, thereby removing the limitation that all prior synchronous CMOS architectures imposed typically on a minimum Vout.

[0039] In the instance of a step-up topology with full disconnection of the load in the shut-down condition, upon startup of the circuit 40, the highest voltage (Vmax) available in the circuit will be:

$$Vmax = Vin;$$

but, since Vout = 0 at steady state, it is:

$$Vmax = Vout < Vin.$$

[0040] A possible example of how the logic circuit 24 can be implemented is illustrated by the detailed block diagram of Figure 5.

[0041] A zero crossing comparator 44 is connected in the circuit 24 to turn off the P-channel power transistor 21 when, in a discontinual mode of operation, the inductor energy is completely deleted during the switching cycle. In this case, the voltage across the inductor would be 0V, and the comparation carried out between the node 32 at a voltage Vlx and a voltage Vbias=Vx generated internally of the biasing circuit 22 and appearing at the node X. This voltage Vbias is given as:

$$Vbias = max(Vin, Vout).$$

[0042] A wiring diagram of a possible implementation of the zero crossing comparator 44, having compatible inputs with Vbias, is shown in Figure 6.

[0043] The P-channel transistor 21 is always turned off when the inductor current is nil (step-up mode).

[0044] The circuit 24 also includes a digital circuit portion 56 adapted to generate short pulses on the trailing edge of the gate voltage of the N-channel MOS power switch transistor 26. This portion 56 comprises a series of two-input logic gates 52, 45, 46 and a series of inverters 47, 48, 49, 50 for feeding the output signal from the last logic gate in the series back to one of the other logic gate inputs.

[0045] The short pulses generated by the circuit portion 56 are used for turning on, in a synchronous manner and with minimized cross conduction, the P-channel power transistor 21, regardless of the value attained by the output of the zero crossing comparator 44 described previously. During the power-off transient of the N-channel transistor 26, the electric potential Vlx at the node 32 is for a short time higher than the output voltage Vout, so that the zero crossing comparator 44 would issue a wrong instruction not to turn on the P-channel transistor 21, thereby causing substantial delay in the turning on of this transistor and penalizing the conversion efficiency of the circuit.

[0046] The logic circuit 24 further includes a drive circuit block 35 which comprises a latch adapted to generate synchronized waveforms for driving the control (gate) terminals of the MOS transistors 21 and 26.

[0047] The latch 35 receives a signal PWM from an external generator 23 and processes this signal through a series of logic gates. The control signal for the transistor 26 is picked up downstream of a first logic gate 36. This signal is then transmitted to the other transistor 21 through a pair of logic gates 37 and 38 of the NOR and AND type, respectively. Furthermore, the output signal from the logic gate 38 is applied to an input of the logic gate 36. The construction of the latch 35 is completed by an inverter 39 and a set of NOR logic gates 41, 42 and 43. The ouput from the gate 38 is applied to an input of the gate 41 via the inverter 3, the gate 42 being input signals issuing from the gate 41, the gate 43 and the logic gate 45 of the pulse generator 56. The gate 43 receives the output from the comparator 44, on one of its inputs, and on the other input, receives a signal issuing from the logic gate 52 of the pulse generator 56 which is also applied to one input of the other NOR gate 41.

[0048] The construction of the logic circuit 24 further comprises a ringing suppression circuit portion 55 which functions to remove the high-frequency oscillations that occur, in the discontinual mode of operation, within the node 32 at the electric potential Vlx in consequence of the power-off transient of the second order circuit formed of the inductor and the parasitic capacitances of the power transistors 26 and 21. The overall effect of the circuit is one of degrading the Q of the oscillating circuit, thus heavily damping the free oscillations.

[0049] The circuit portion 55 comprises a logic gate 54 and an output stage 53 consisting of a pair of P-channel MOS transistors which operate to suppress ringing by short-circuiting the inductor. These transistors are provided in a back-to-back configuration in order to prevent their body-drain junctions from being turned on during the power-on time period (Ton) or the power-off time period (Toff) of the waveform PWM that establishes at the node 32.

[0050] Thus, the proposed circuit distinguishes itself from prior synchronous rectifier architectures, overcoming their limitations and affording the following advantages:

a step-up DC-to-DC conversion of very high efficiency (typically 90-95%);

deactivation of the P-channel 21 parasitic diode;

operability starting from very low supply voltages (0.8V);

suppression of the high-frequency ringing that typifies switching regulators in the discontinual mode of operation;

very low standing current consumption (typically 8μA).

Claims

1. A synchronous CMOS rectifying circuit for step-up devices, of the type which has at least one input terminal (IN) and one output terminal (OUT), and is adapted to convert a DC input voltage (Vin) to a DC output voltage (Vout), comprising:

   an inductor (L) for transferring energy from said input terminal (IN) to said output terminal (OUT);

   a first electronic switch (26) for coupling the inductor (L) to the DC input voltage (Vin);

   a second electronic switch (21) for coupling the inductor (L) to the output terminal (OUT);

   characterized in that the second electronic switch (21) is a MOS power transistor and has a first conduction terminal connected to a terminal of the inductor (L), and has a second conduction terminal coupled to the output terminal (OUT) of the rectifier, said transistor (21) being driven by a control logic circuit (24) effective to sense the difference in electric potential between at least one conduction terminal (32) of said transistor and the body terminal (X) of said transistor.

2. A circuit according to Claim 1, characterized in that it further comprises a capacitor (C) connected to the output terminal (OUT) for storing energy being transferred from the inductor (L).

3. A circuit according to Claim 1, characterized in that the control logic circuit (24) comprises:
   a drive block (35) for driving the first switch (26) and the power transistor (21), and a compare block (44) arranged to sense the difference in electric potential across said conduction terminal (32) and said body terminal (X), and to supply an enable signal to the drive block (35).

4. A circuit according to Claim 3, characterized in that the compare block (44) enables the drive block (35) upon the electric potential (Vlx) at the first conduction terminal (32) rising above the electric potential (Vx) at the body terminal (X).

5. A circuit according to Claim 3, characterized in that the control logic circuit (24) further comprises a digital generator (56) of short pulses for turning on the power transistor (21) synchronously during the power-off transient of the first switch (26).

6. A circuit according to Claim 3, characterized in that the drive block (35) is a logic gate latch arranged to generate synchronized waveforms.

7. A circuit according to Claim 3, characterized in that the control logic circuit (24) further comprises a ringing suppression circuit portion (55) having an output stage (53) formed of PMOS transistors.

8. A circuit according to Claim 1, characterized in that the electric voltage potential (Vx) at said body terminal (X) of the power transistor (21) is supplied from a biasing circuit (22) which receives the input voltage (Vin) and the output voltage (Vout) to generate a bias voltage (Vx) at the body terminal (X) corresponding to the highest voltage available in the circuit.

9. A circuit according to Claim 1, characterized in that the power transistor (21) is a PMOS transistor.

10. A method of providing a DC/DC conversion between a DC input signal (Vin) presented on an input terminal (IN) and a DC output signal (Vout) presented on an output terminal (OUT) of a converting/rectifying circuit. comprising:

an inductor (L) for transferring energy from said input terminal (IN) to said output terminal (OUT):

a first electronic switch (26) for coupling the inductor (L) to the DC input voltage (Vin):

a second electronic switch (21) for coupling the inductor (L) to the output terminal (OUT):

characterized by using a MOS power transistor as the second switch (21). and sensing the difference in electric potential between at least one conduction terminal (32) and the body terminal (X) of the MOS power transistor so that the transistor (21) can be driven according to said difference in electric potential.

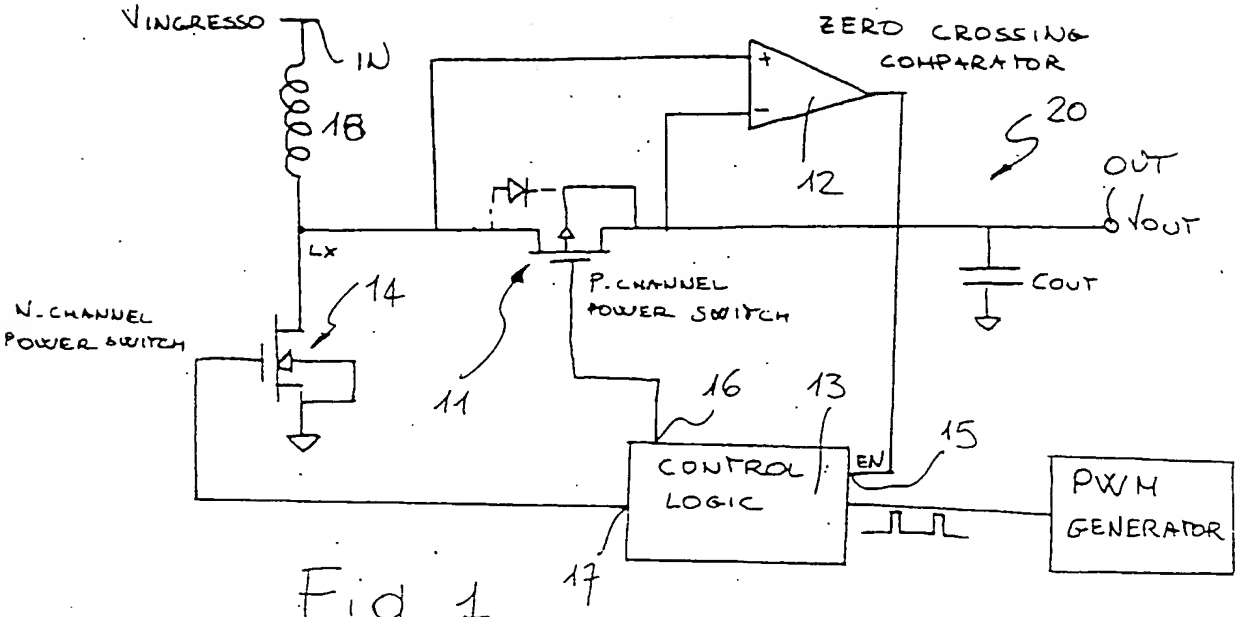
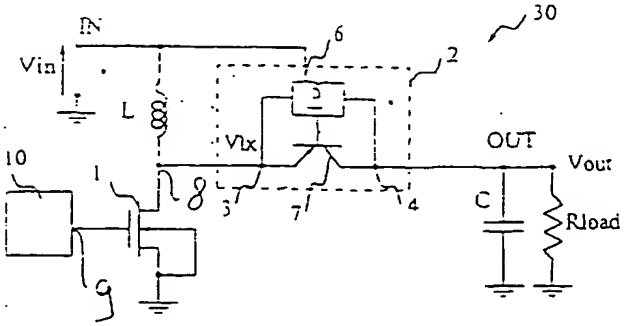


Fig. 1

PRIOR ART

Fig. 2

PRIOR ART



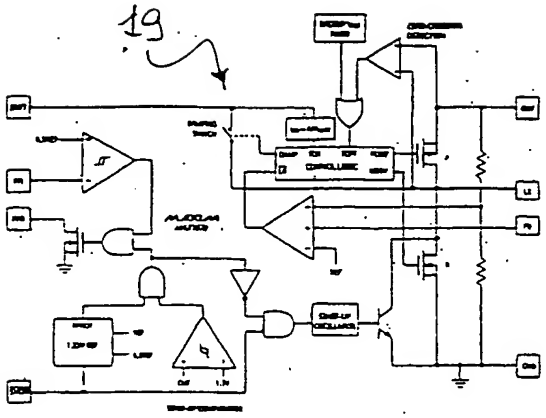


Fig. 3

PRIOR ART

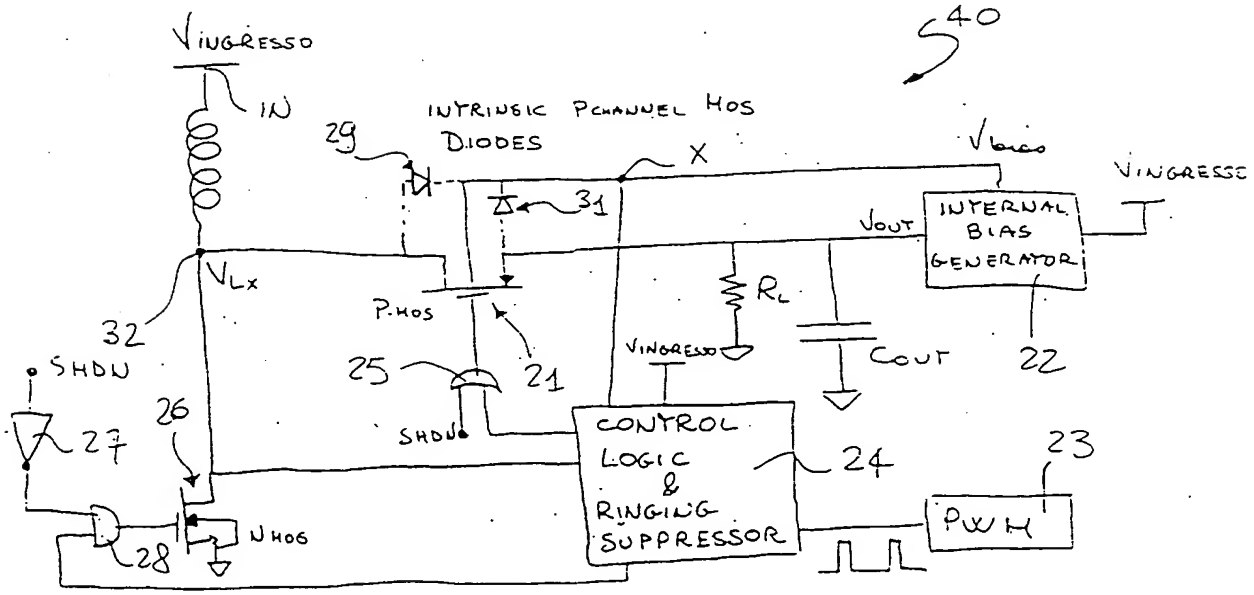


Fig. - 4

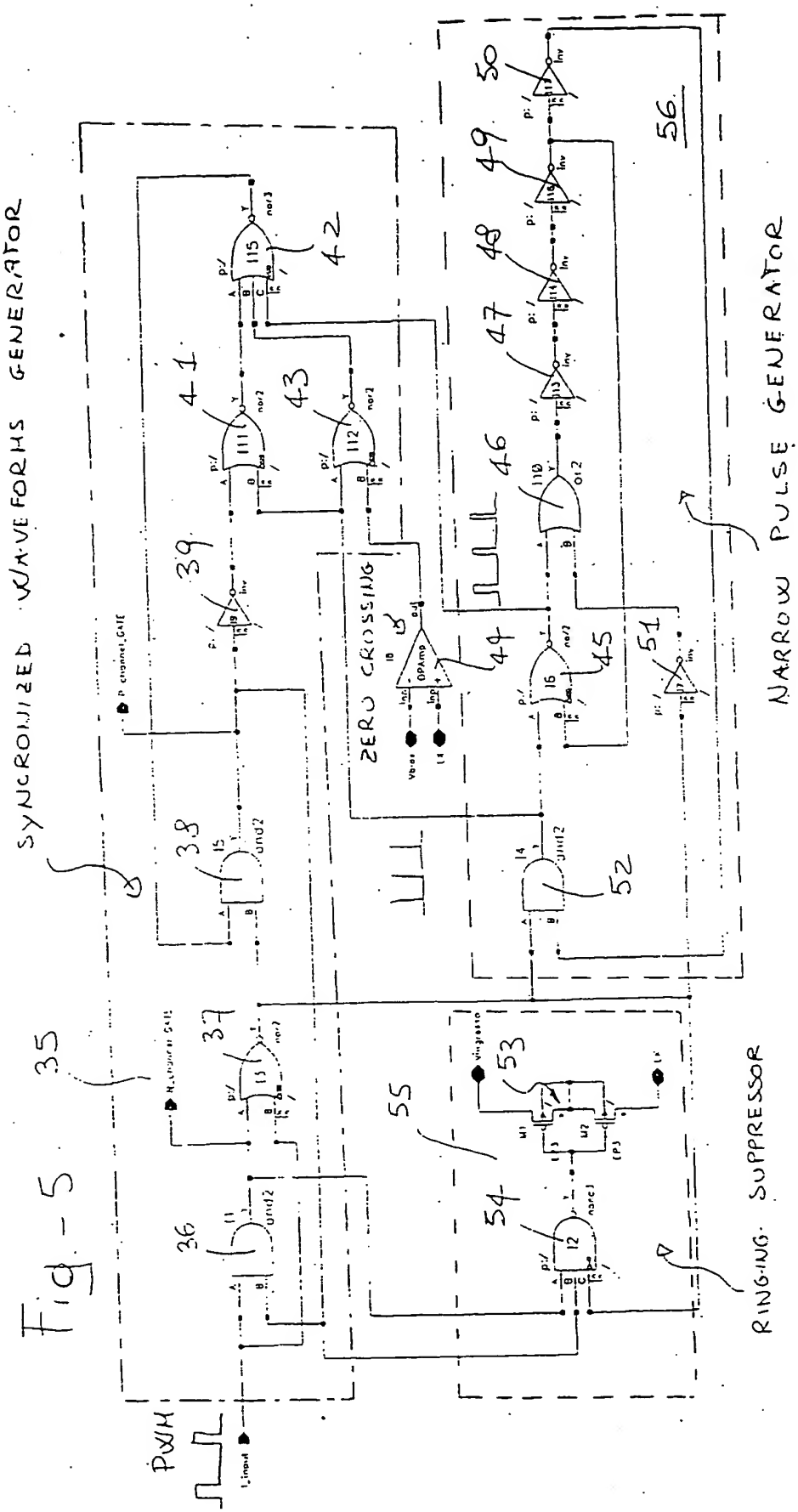

SYNCROIJIZED WAVEFORMS GENERATOR
ZERO CROSSING
NARROW PULSE GENERATOR
RINGING SUPPRESSOR
PWM
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Fig - 5

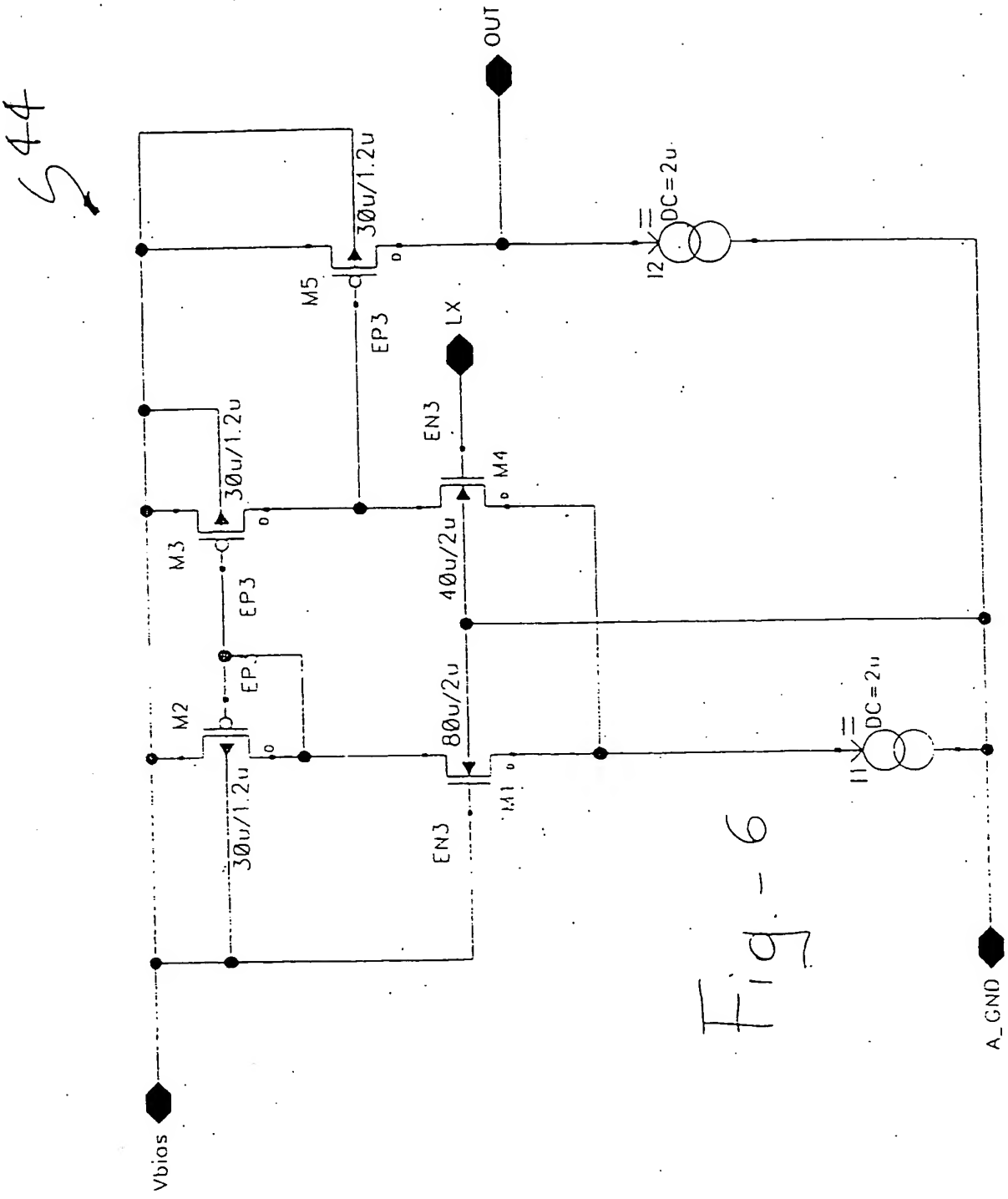

S44
OUT
30u/1.2u
M5
EP3
LX
EN3
M4
40u/2u
I2
DC=2u
30u/1.2u
M3
EP3
EP2
M2
80u/2u
I1
DC=2u
30u/1.2u
EN3
M1
Vbias
A_GND

Fig-6

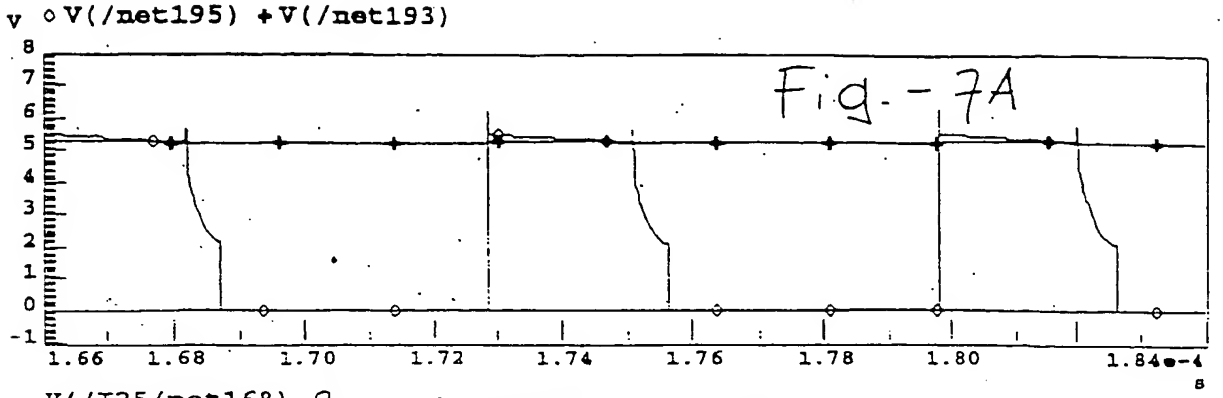


Fig. - 7A

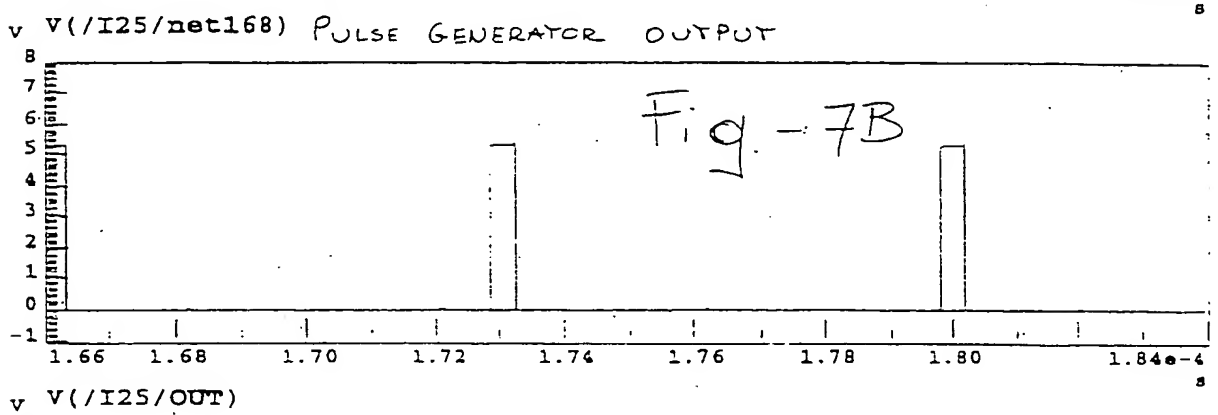


Fig. - 7B

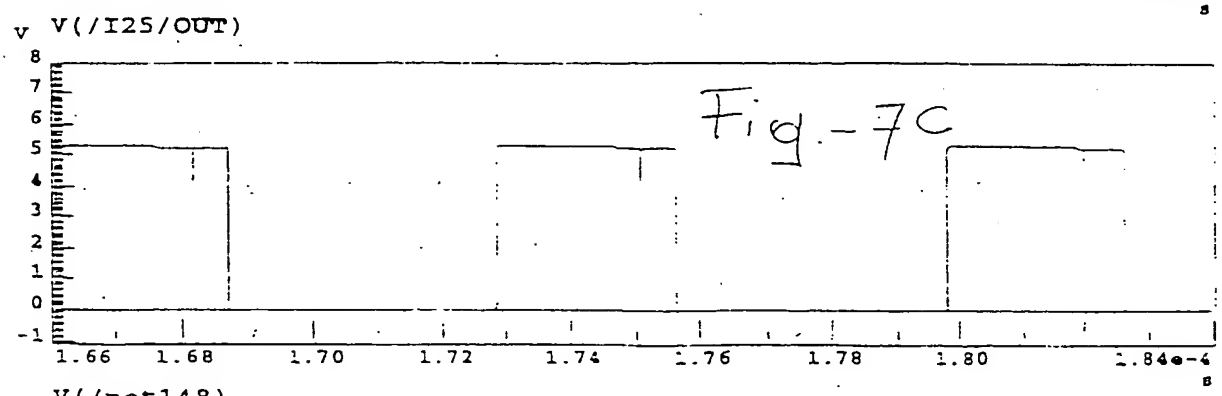


Fig. - 7C

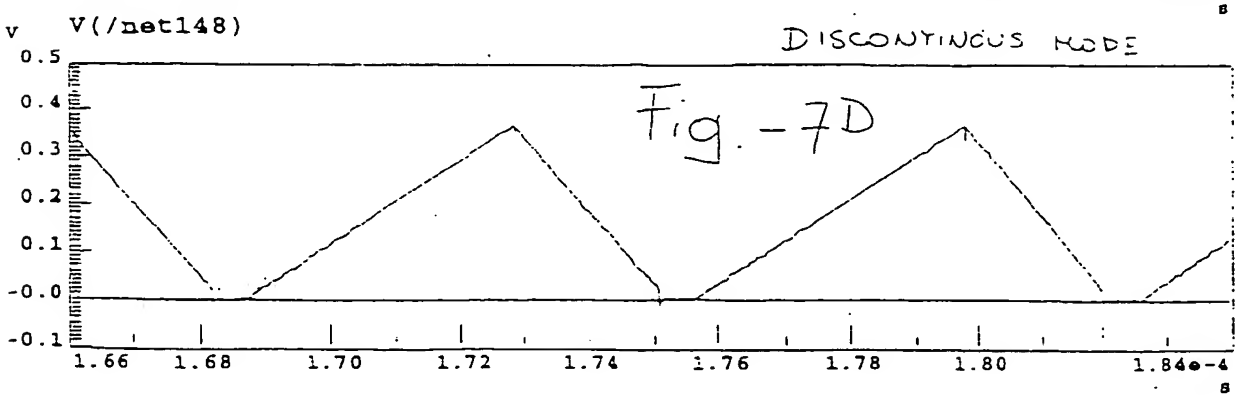


Fig. - 7D

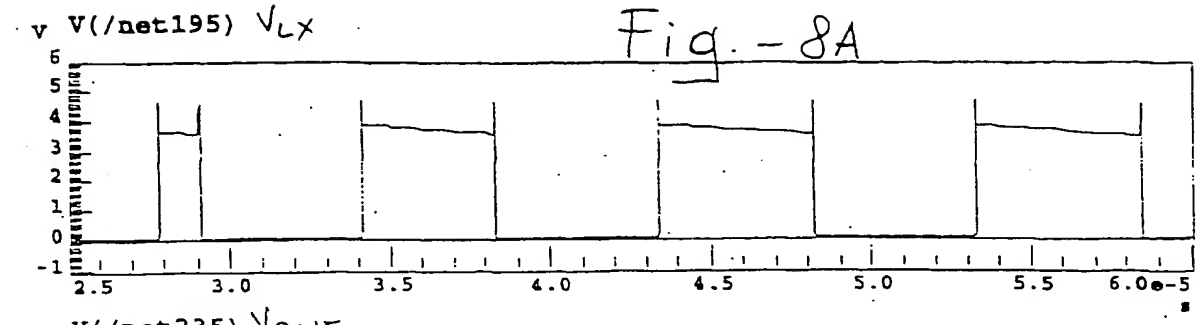


Fig. - 8A

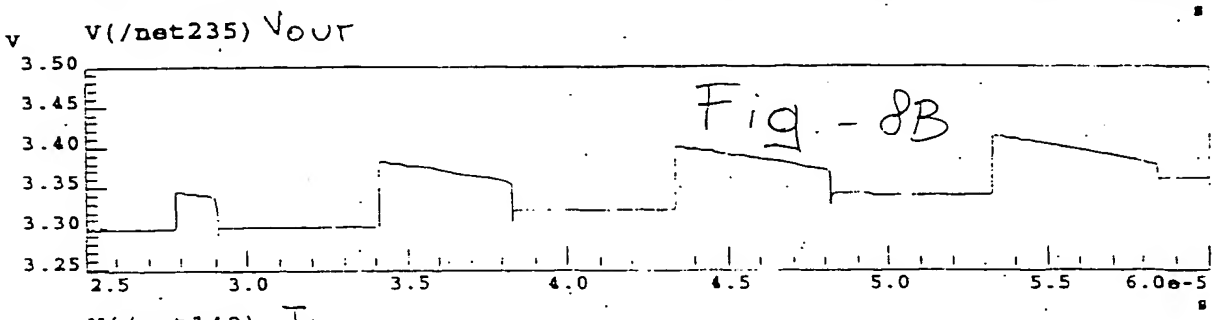


Fig. - 8B

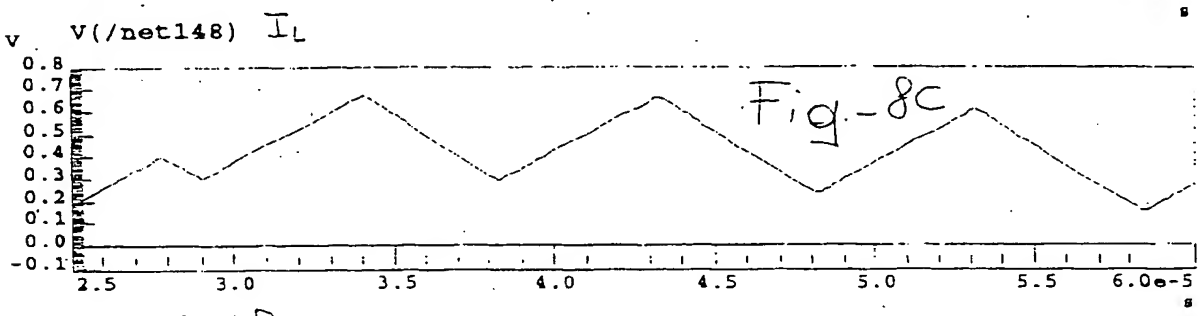


Fig. - 8C

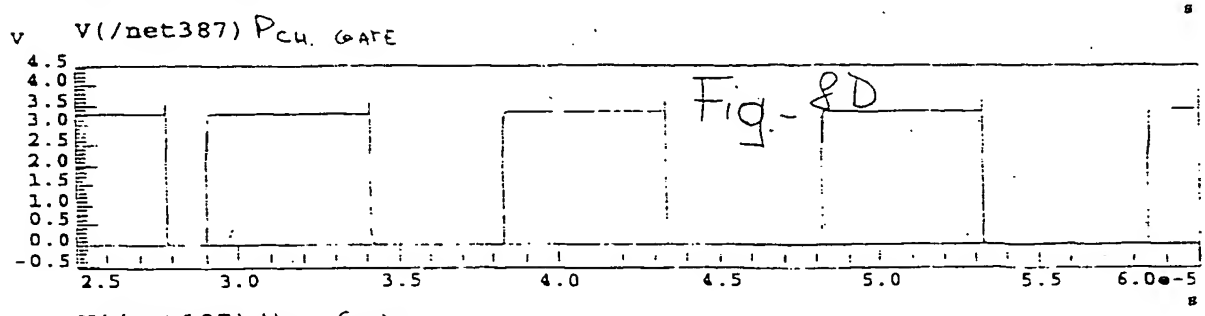


Fig. - 8D

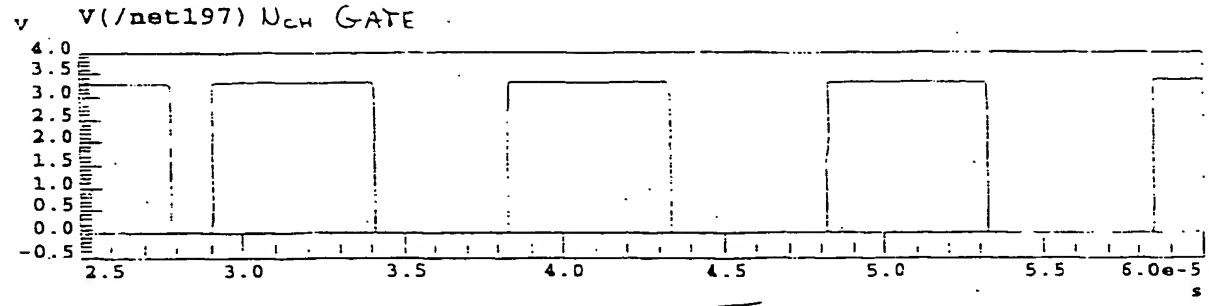
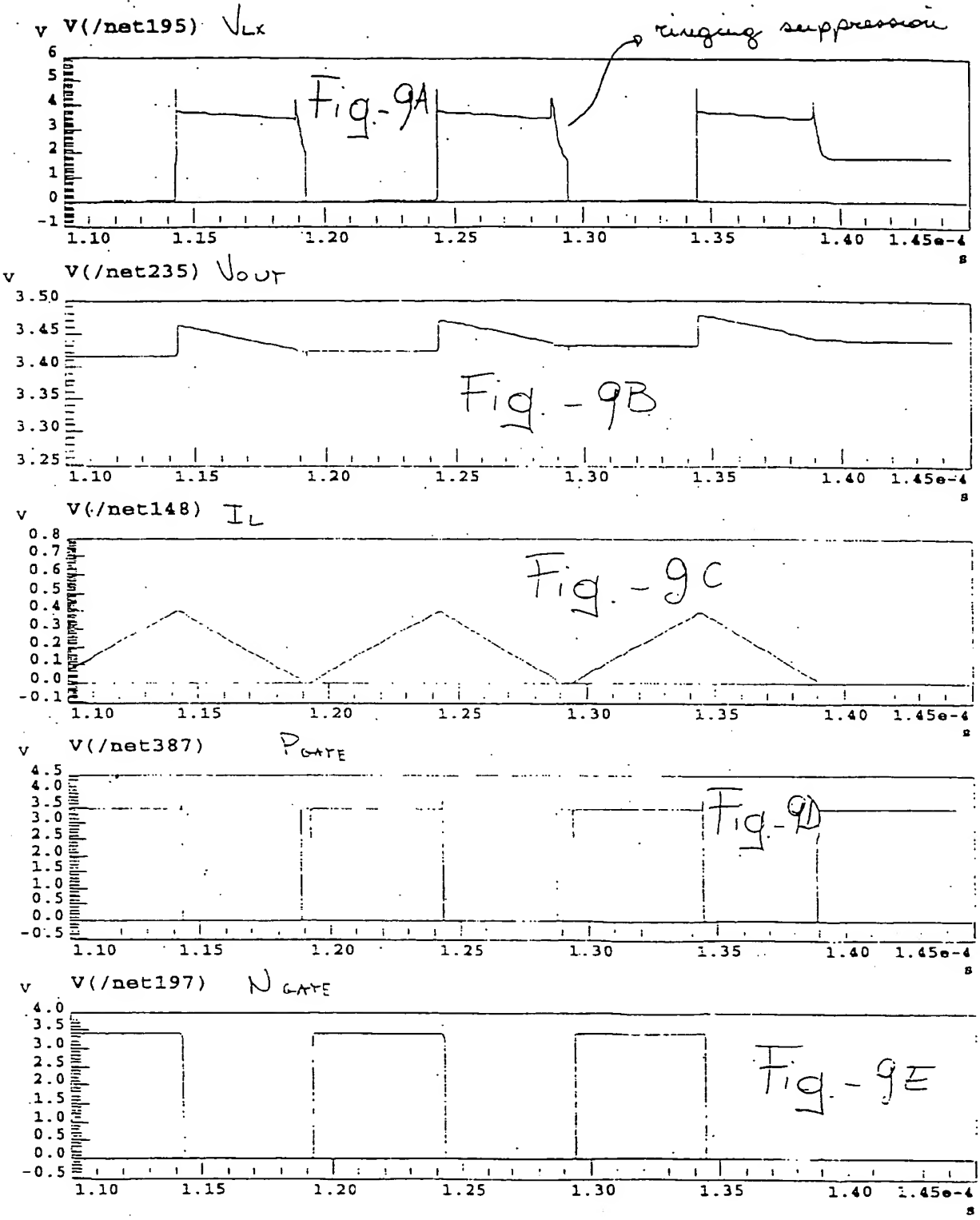


Fig. - 8E


V V(/net195) VLX
ringing suppression
Fig.-9A
V V(/net235) VOUT
Fig.-9B
V V(/net148) IL
Fig.-9C
V V(/net387) PGATE
Fig.-9D
V V(/net197) NGATE
Fig.-9E
1.10 1.15 1.20 1.25 1.30 1.35 1.40 1.45e-4
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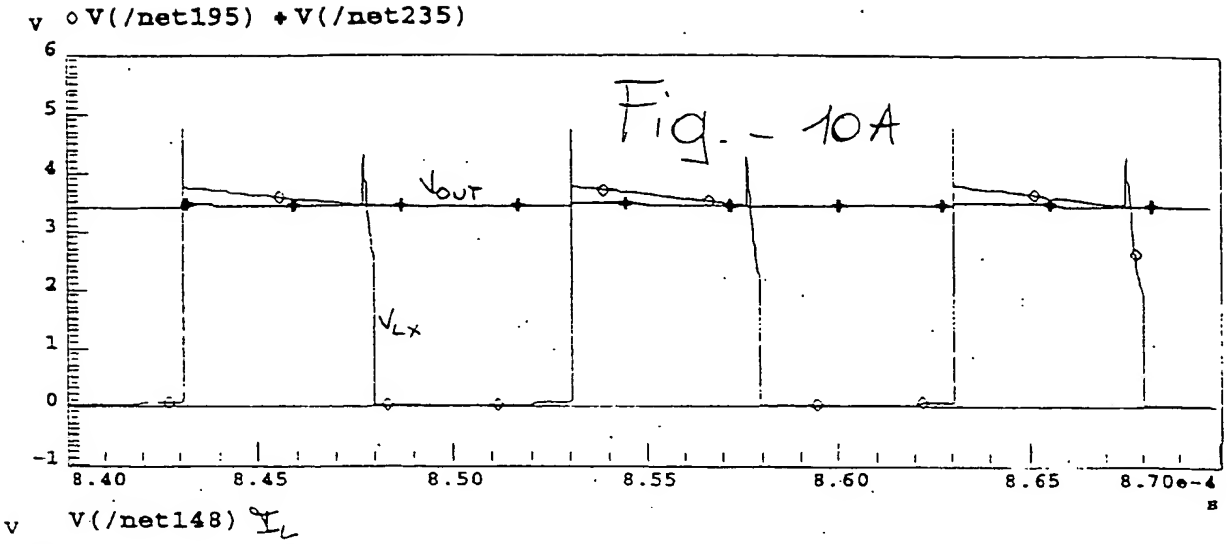

Fig. - 10A

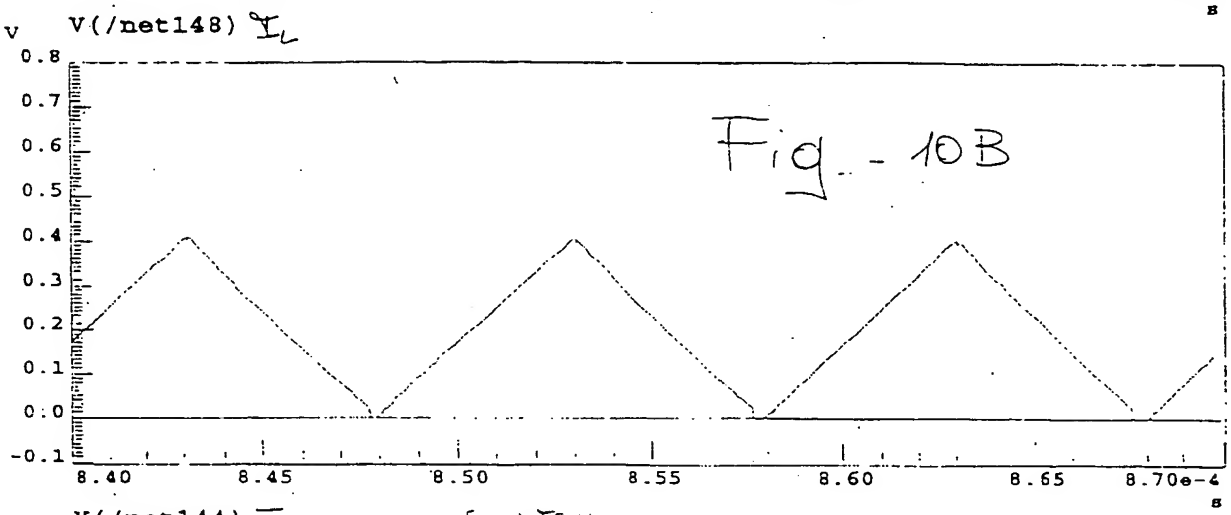

Fig. - 10B

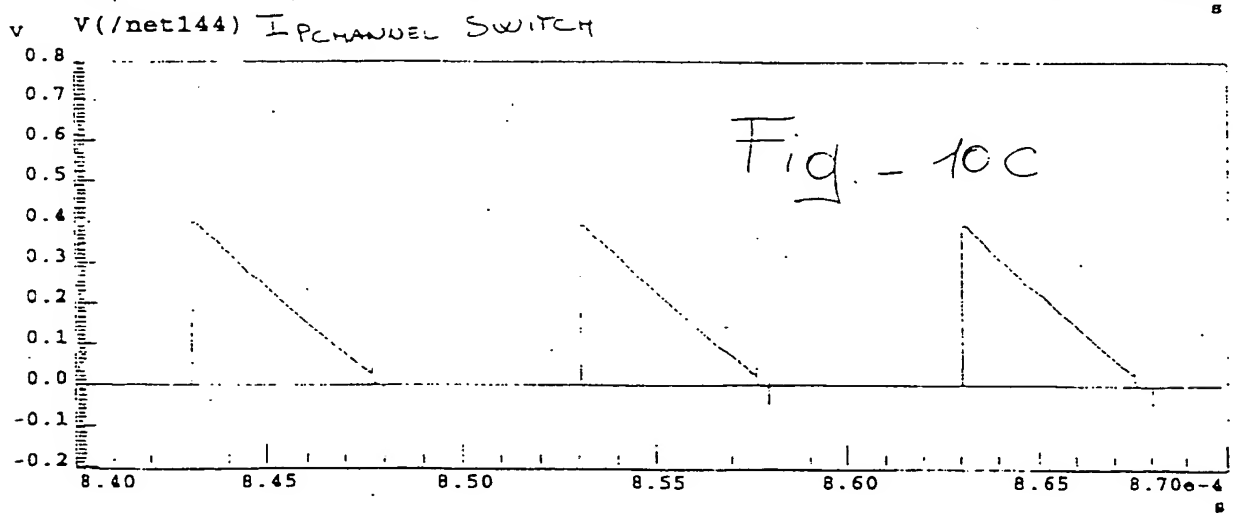

Fig. - 10C

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0432

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 751 139 A (HACK THOMAS PETER ET AL) 12 May 1998 (1998-05-12) * figure 4 *	1,10	H02M3/158
A,D	"MAX 1678: 1-Cell to 2-Cell, Low-Noise, High Efficiency, Step-Up DC-DC Converter" MAXIM INTEGRATED PRODUCTS - DATASHEETS, [Online] July 1998 (1998-07), XP002130025 Retrieved from the Internet: <URL:http://www.maxim-ic.com> [retrieved on 2000-02-08] * the whole document *	1-10	
T,D	EP 0 933 865 A (ST MICROELECTRONICS SRL) 4 August 1999 (1999-08-04) * the whole document *	1-10	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H02M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 February 2000	Lampe, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
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L : document cited for other reasons

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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 83 0432

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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08-02-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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